Code No: B5506, B5703 **NR**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II SEMESTER EXAMINATIONS, APRIL/MAY 2012
LOW POWER VLSI DESIGN
(COMMON TO EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) How are the CMOS logic gates classified? Explain.
b) Give the complete flow for Analog IC design and explain about feature size and VOD variation in chip design.

2. What are the different Isolation techniques used in BICMOS IC fabrication? Explain using necessary sketches.

3.a) Explain about short channel effect.
b) What are the advantages with the productions of graded Drain Structure?

4. Explain about different design considerations for Base, Emitter and Collector in the case of BJT processing.

5.a) Give the structure for Poly Silicon Emitter High performance BICMOS circuit and explain about the same.
b) Discuss about the advantages and disadvantages of Copper Interconnects for deep submission CMOS / BICMOS structures.

6.a) Explain about BSIM, IGFET Model and EKV models for MOSFETS.
b) Compare different types of SPICE MOSFET models.

7.a) Draw the circuit for Full Swing complimentary MOS / Bipolar logic circuit for two input NAND gate and explain its operation.
b) Draw the circuit for High performance complimentary coupled BICMOS three input NAND and explain its working.

8. Write notes on any TWO
a) Limitations of MOSFET Models
b) Low Power latches
c) Quality measures for latches and Flip – Flops

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